IN THE U.S. PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/626,760
Applicant	:	Joshi, Rajiv V. et al.
Filed	:	July 21, 2003
TC/AU	:	2818
Examiner	:	Nguyen, Thinh T.
Docket No.	:	909A.0128.U1(US)
Customer No.	:	29683
Title	:	FET CHANNEL HAVING A STRAINED LATTICE STRUCTURE ALONG MULTIPLE SURFACES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. § 1.131

1. We, Rajiv V. Joshi and Richard Q. Williams, hereby attest that we are jointly the first inventors of the invention described and claimed in the above-referenced patent application now pending before the U.S. Patent Office. Exhibits A through H described below and attached hereto represent our own work or characterizations of our own work as described in that patent application during the times indicated.

2. Exhibit A is a copy of one page of a graphical presentation that illustrates a cross section of a strained silicon channel of a field effect transistor FET that is in contact with a relaxed SiGe layer. Exhibit B is a copy of two non-sequential pages of a single email sent to inventor Joshi, among others. Exhibit B summarizes a meeting in which testing for strained silicon FETs was explored, and specifically notes at item "(5) Test Sites – SRAM sites" that inventor Joshi presented materials to the group. Inventor Joshi hereby attests that those materials included Exhibit A. Exhibits A and B are dated July 2001.

3. We conceived of the invention in the United States as described and claimed in the above-referenced application at least as early as September 20, 2001, as evidenced by Exhibit C. Exhibit C includes numbered pages 1, 7 and 8 of a presentation entitled "Iceland10S2" describing strategies for testing embodiments of the invention, a finFET with strained silicon along dual gates.

4. Exhibit D is a copy of an email in two pages dated August 9, 2002 from inventor Joshi searching for alternative test sites for evaluating embodiments of the strained FinFET invention.

4. Exhibit E is a copy of an email in two pages dated November 7, 2002, informing recipients, including inventor Joshi, of a meeting to discuss the ICELAND test site, showing the inventor's continued efforts to subject the strained FinFET invention to actual testing.

5. Inventor Joshi took approximately three weeks vacation during December 2002.

6. Exhibit F is a copy of a one-page email between the inventors dated January 24, 2003, wherein 'put this in' refers to submitting an invention disclosure report describing the strained FinFET invention to a patent review committee within IBM for consideration for filing a patent application.

7. Exhibit G is a copy of three pages of an invention report prepared by the joint inventors and dated January 31, 2003. This was submitted to IBM for the purposes of evaluating the invention for patent protection.

8. Exhibit H is a copy of three pages of an email dated Feb. 27, 2003 that was sent to inventor Joshi, among others, confirming a meeting to discuss design, testing, and delivery of various IBM projects, including the strained FinFET invention, and indicates inventor Joshi's continued activity on the invention.

9. I hereby attest that the Exhibits cited herein are true copies, with the exception of the footers of Exhibit C, which are overwritten with dates of which they were recently copied from archives. Redacted portions include materials not original to the true documents, phone numbers and email addresses of other individuals, and other material not relevant to showing conception or diligence. Each of the undersigned hereby acknowledges that the statements made herein are true or are made on information and belief that is believed to be true. Each of the undersigned further acknowledges that any willful false statements are punishable by fine or imprisonment, or both, in accordance with 18 U.S.C. § 1001; and that such false statements may jeopardize the validity of any patent that may issue form the application to which this Declaration pertains.

Respectfully Submitted,

Rajiv V. Joshi

Rajiv V. Joshi

March 8, 2005

Date

Richard Q. Williams

Date

Notary Seal and date:

Jennifer A Smith 3/8/05

JENNIFER A. SMITH
Notary Public, State of New York
No. 01SM5063001
Qualified In Westchester County
Commission Expires July 15, 20 06

FAX: 263-944-0243

IN THE U.S. PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/626,760	TC/AU	:	2818
Applicant	:	Joshi, Rajiv V. et al.	Examiner	:	Nguyen, Thinh T.
Filed	:	July 21, 2003	Docket No.	:	909A.0128.U1(US)
Title	:	FET CHANNEL HAVING A STRAINED LATTICE STRUCTURE ALONG MULTIPLE SURFACES			

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. § 1.131

1. I, Richard Q. Williams, hereby attest that Rajiv V. Joshi and myself are jointly the first inventors of the invention described and claimed in the above-referenced patent application now pending before the U.S. Patent Office.

2. Exhibit F is a copy of a one-page email between the inventors dated January 24, 2003, wherein 'put this in' refers to submitting an invention disclosure report describing the strained FinFET invention to a patent review committee within IBM for consideration for filing a patent application.

3. Exhibit G is a copy of three pages of an invention report prepared by the joint inventors and dated January 31, 2003. This was submitted to IBM for the purposes of evaluating the invention for patent protection.

4. I hereby attest that the Exhibits cited herein are true copies. Redacted portions include materials not original to the true documents, phone numbers and email addresses of other individuals, and other material not relevant to showing conception or diligence. I hereby acknowledge that the statements made herein are true or are made on information and belief that is believed to be true. I further acknowledge that any willful false statements are punishable by fine or imprisonment, or both, in accordance with 18 U.S.C. § 1001; and that such false statements may jeopardize the validity of any patent that may issue form the application to which this Declaration pertains.

Respectfully Submitted,

Richard Q. Williams — Richard Q. Williams

3/8/2005 — Date

Notary Seal and date:

{PAGE }

SS CMOS Device Expt.: Process Flow

-
-

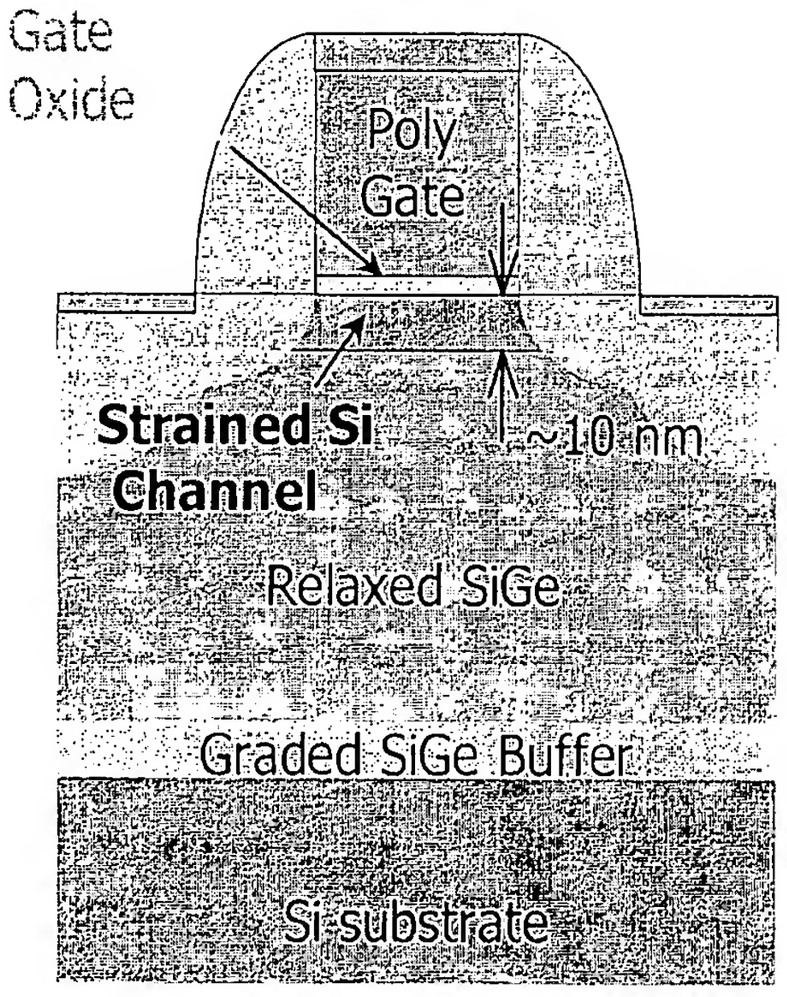


Exhibit A

Ching-Te Chuang

07/24/2001 01:21 PM

To: , , , Joshi/Watson/

cc:

From:

Subject: *IBM Confidential: Summary & Action Items of CMOS11S Strained Si Devices Meeting on 7/19/2001

Dear Strained Si Device Team Members:

Below please find the summary of the meeting on CMOS11S strained Si devices on 7/19/2001 (10:30 - 11:30, Room 27-223, YKT).

Please notice: (1) Discussion and action items are embedded under each item,
(2) Meeting time/location for our next meeting on 8/02/2001
(3) We should focus our effort in test site related actions at present and in the near future

Discussion Items for Strained Si Devices Meeting (7/19/2001)

(1) Logictics: Regular Meeting/Tele-Con ? When ? How Often ?

Discussion: Thomas Ludwig is coming to U.S. first week of 08/01. We'll set up meeting on Thursday 8/02/2001 for detailed discussion
of test site related issues and future meetings.

Action : Meeting Set-Up

Exhibit B

(5) Test Sites - SRAM sites

- Existing SRAM cells & sense amp sites on ALTA
- Existing SRAM sites on ICELAND10S (No existing SRAM site on ICELAND10S)
- Cell Beta ratio ?
- Cell layout orientation effect ?
- Dense layout effect ?
- Modified or new sites ?

Discussion: Rajiv Joshi showed the schematics and layout of single-port and dual-port cells.

Action: Rajiv Joshi and Steven Kowalczyk, working with people listed in item (4) and based on the outcome of Item (4) action item, to come up with list/proposal for SRAM sites.

(6) Test Sites - Strained Si device specific sites

Exhibit C

ICELAND10S2

Chiplet on BEACON

Thomas Ludwig
Future Product Technology
IBM Boeblingen, Germany

Proposal

- design experiments if possible with both technologies in mind:
  - strained Silicon
  - FinFET Dual Gates
    - this will saves real estate and make the experiments multipurpose
- Methodology:
  - design the experiments for Strained-Si and add the additional layout masks for FinFET,

s-parameter Experiments

- s-parameter FET structures
- s-parameter Wiring structures

  - together gives us the whole picture and the confidence that the probing environment does not influence the measurement results

Aug 9, 2002

Mike Gonzales,

FOllowing macros views are copied in your public.
(these macros exist in my library rvj_beacon2_SiGe
I have copied my macros in your public.
These are
1. rvj_sramHF2_mac -

PLEASE PROVIDE THE 10S PADS replacing the OLD PADS.

2. rvj_sramHF3_mac - New circuitry to improve timing using local clock
PLEASE PROVIDE THE 10S PADS replacing the OLD PADS.

In addition you have following old macros. I need them to be put on.

1. rvj_trgateTemp10s.gl1 - This macro was implemented on earlier ALTA testsite

Exhibit D

2. rvj_sram1EF.gl1

This macro evalautes performance, stability, timing and leakage and power of standard and thin cell from pokalliance 9s library. The thin cells, bsel and sense amp are modified to suit 10s design.

3. rvj_sramHF_mac.gl1

;
It also shows how to adjust the sae signal with respect to delayed clock.
PLEASE PROVIDE THE 10S PADS replacing the OLD PADS.

4. rvj_m1m4_xsec.gl1(Dec 22, 01)

Please provide the standard 10s pad replacing the old pads.

Thanks for all your help.

R. V. Joshi

11/07/2002 10:30 AM Local Time

11/07/2002 11:30 AM Local Time

Title:

CMOS11S ICELAND Test Site Meeting
CR 27-223, Yorktown

Location:

-No room information available-

Chair: Ching-Te Chuang/Watson/IBM

To (required):

Joshi/Watson/

cc (optional):

Exhibit E

(1) ICELAND Test Site Logistics (Deadlines, Design Lib./Delivery, etc.) - Thomas Ludwig
(2) Site Design Status - All

USA Toll Free Number:
International Number: +
PASSCODE:

----- Forwarded by Richard Q Williams/Burlington/IBM on 02/08/05 05:45 PM -----

Richard Q Williams/Burlington/IBM

01/24/03 04:45 PM

To
R Joshi/Watson/IBM
cc

Subject
finfet disclosure

Hi,

I think if we want to put this in, we should put it in right away.

I think they are not far from the idea of building this in fins, even if there is no mention yet of strain (that I know of). I think that we shouldn't wait for simulation :

Time is critical here.

Richard

Richard Williams
IBM Microelectronics

Exhibit F

YOR9-2003-0073

Disclosure YOR8-2003-0049

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By R Joshi On 01/31/2003 07:23:53 PM EST
Last Modified By wpts1 wpts1 On 02/28/2003 10:42:01 AM EST

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**
STRAINED SiGe FINFETS (SSGFins)

Summary

Status		Under Evaluation
Final Deadline		
Final Deadline Reason		
*Processing Location		Yorktown
*Functional Area	select	(802) 802 VLSI/Circuit Design
Attorney/Patent Professional		Louis J Percello/Watson/IBM
IDT Team	select	Kevin Warren/Watson/IBM Louis J Percello/Watson/IBM
Submitted Date		01/31/2003 07:30:35 PM EST
*Owning Division	select	RES
Incentive Program		
Lab		
*Technology Code		140H
*PVT Score		

Inventors with a Blue Pages entry

Inventors: R Joshi/Watson/IBM, Richard Q Williams/Burlington/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Joshi, Rajiv V. Williams, Richard Q.				

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection

Attorney/Patent Professional	Louis J Percello/Watson/IBM
IDT Team	Kevin Warren/Watson/IBM Louis J Percello/Watson/IBM
Response Due to IP&L	03/03/2003

Exhibit G

R.V. Joshi (Serial 917860) R.Q. Williams (Serial 509041)

Title of Invention: STRAINED SiGe FINFETS (SSGFins)

Field of the invention

The present invention generally relates to the device design and fabrication of highly-strained SiGe FINFET structures on a semiconductor integrated circuit chip.

BACKGROUND

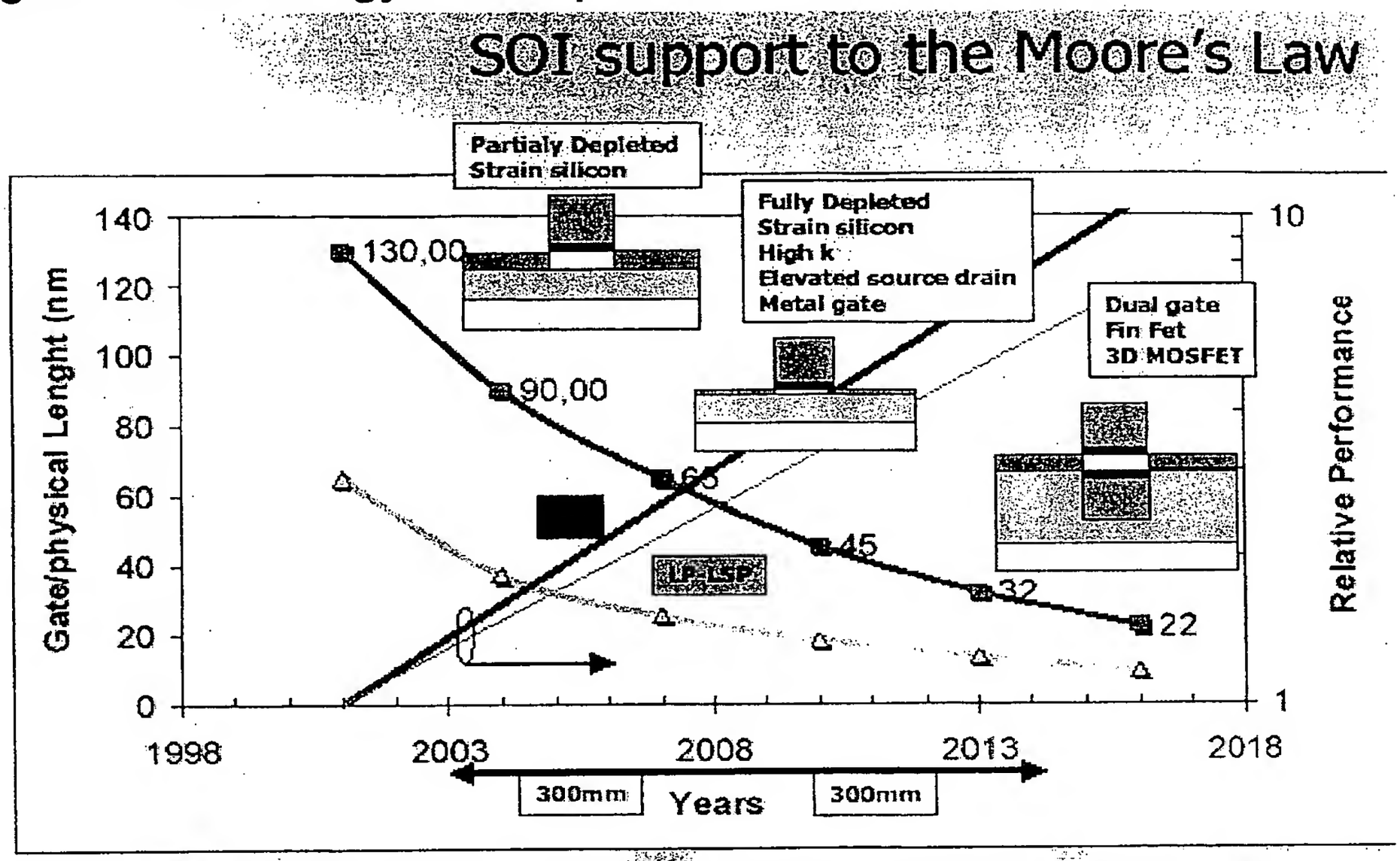
The technology scaling continues as we approach the "red brick wall" with respect to future technology generations – the color red is used to indicate technology nodes where some of the device design features are undefined. Some of the major and apparent problems in technology scaling are excessive gate leakage currents, which directly affect standby power, higher active power and improvement in performances at the cost.

The technology roadmap from the research perspective is given in Fig. 1. To alleviate the gate leakage current problems, lateral scaling is a feasible option. however this does not yield significant performance improvement or improve the off current situation. One possible future technology is strained silicon/SiGe – on-insulator, which has received wide attention recently. Due to the lattice mismatch, a pseudomorphic layer of Si is under biaxial tensile strain. The strain modifies the band structure and enhances carrier transport. It has been reported that the mobility enhancement for nfets is 70% while it is only 20-30% for pfets. Double gate structure are also attractive because they are scalable. What is needed is the solution to both scaling and enhanced performance for both pfet and nfets.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide enhanced device performance in a scalable device structure. It is another objective of the invention to improve device mobility while being relatively easy to incorporate in the circuit applications.

Figure 1: Technology roadmap.



Embodiments

1. Unstrained NFET FIN with Strained SiGe PFET FIN

2. Strained-Si NFET with Unstrained PFET FIN
Changing the crystal orientation to (110) can be used to enhance the based PFET performance. The disclosed method works best in chip designs with moderately large islands of N devices and P devices.

Other silicon hetero-materials (e.g., silicon germanium carbides) can be used to induce strain in the appropriate structures.

3. A vertical separator/buffer made on TEOS (STI) can be included between the SiGe and the Si if needed (an option).

4. Finfets made up of strained Si and relaxed SI-Ge layers. Sharp corners introduce more tensile strains into the fins.

Ching-Te Chuang

02/27/2003 08:42 AM

To: R Joshi/Watson/I

cc:
From:
Subject: *IBM Confidential: Fw: Denali/Homer/ICELAND T1 Testchip Meeting For 02/28 - Please call in

Gents:

Please call-in. This is to dicuss your design status and the delivery schedule.

Thanks !

Ching-Te Kent Chuang

Yorktown Heights, NY 10598
Tel:
Fax:
e-Fax:
E-mail:

Exhibit H

----- Forwarded by Ching-Te Chuang/Watson/IBM on 02/27/2003 08:36 AM -----

Arnold Barish

02/26/2003 08:51 PM

To:

Joshi/Watson/

cc:

From: Arnold Barish/
Subject: Denali/Homer/ICELAND T1 Testchip Meeting
For 02/28

To All:

There is a C11S Denali/Homer/ICELAND test chip meeting this Friday 02/28 from 10:30AM -12:00PM EDT (B705 2H05 for Pok attendees).

This week I want to assess the schedule impact of the latest GR changes found on the crystal server (: on each of your experiments.

I have attached time estimates for each topic for those of you who are unable to attend the entire meeting. Please place any pertinent presentation material out in the teamroom I have scheduled an e-meeting (Meeting Name:T1 Test Chip , full e-meeting details including a link to the meeting can be found at the bottom of this note.

Call in number if you don't have it is:

Domestic
Internat'l
Participant passcode